Design and Analysis of three basic OP AMP

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Ⅰ. Introduction

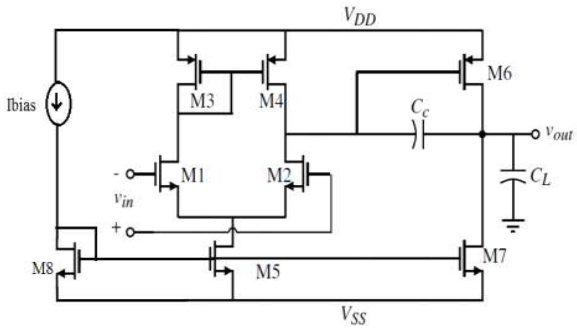
지난 5주간 (2019.01.02. ~ 2019.02.07.) op amp에 대해 Razavi 'Design of Analog Cmos Integrated Circuit' 교재로 학습하였습니다. 이후 2주간 (2019.01.08. ~ 2019.02.20.) two stage op amp, folded cascode op amp, widebandwidth op amp 등 3개의 op amp를 design 하였습니다. 각 amp는 g_m/i_d methodology를 이용하여 주어진 specification을 만족시키기 위해 hand calculation 하였습니다. 이후 350n 공정에서 hspice로 parameter들을 simulation을 하였고 optimization을 거쳐 design을 마쳤습니다.

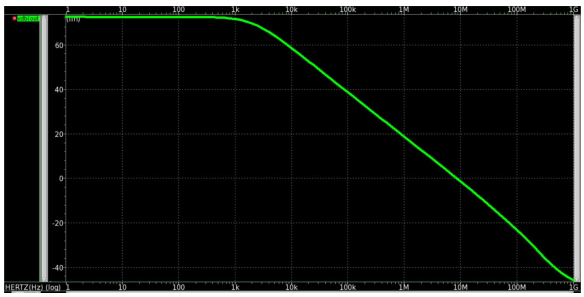
Ⅱ. Two stage op amp

2-1 Target and result of Specification

Parameter	Target	Achievement
DC Gain	≥70dB	72.6dB
Common-Mode Input Range	1V	at least 2V
OutputSwing	1V	2.7V
PowerDissipation (excludebiasing)	100uW	98uW
Unity GainFrequency	8MHz	8.6MHz
Settling Time (0.5V OutputStep)	100nsec to 0.1%	104nec
CMRR at DC	≥70dB at DC	72.6dB
PSRR	≥70dB at DC	82.6dB
Load Capacitance	1pF	1pF
Supply Voltage	3.3V(VDD), 0V(VSS)	3.0V(VDD), 0V(VSS)
Phase Margin	60 °	67.5 °

2-2 Design and Hand calculation





Two stage op amp는 위와 같이 design 하였다. 350nm 공정에서의 Nmos와 Pmos의 $u_n cox$의 값을 가지고 g_m/i_d methodology를 이용하였다. g_m/i_d를 통하여 Vod를 $100mv$로 설정한 후 w/l를 구하고 m, r, c의 값을 추후 다른 spec에 맞도록 계산한 후 결정하였다.

그 결과 parameter들이 아래와 같이 결정되었다.

M1	l=0.55u w=0.4u m=3	M2	l=0.55u w=0.4u m=3
M3	l=0.55u w=0.4u m=9	M4	l=0.55u w=0.4u m=9
M5	l=0.55u w=0.4u m=6	M6	l=0.55u w=0.4u m=54
M7	l=0.55u w=0.4u m=18	M8	l=0.55u w=0.4u m=4
c_c	0pF	c_L	1pF
V_{DD}	3V	V_{ss}	0V
Ibias	5.5uA	R_f	0Ω
vin1	1V	vin2	1V

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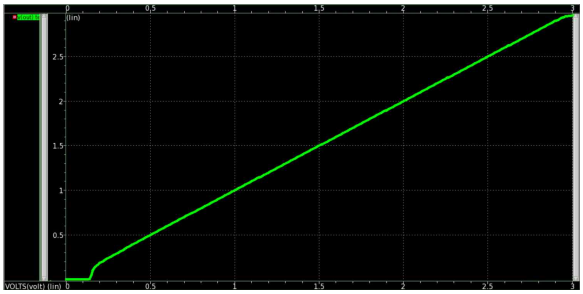
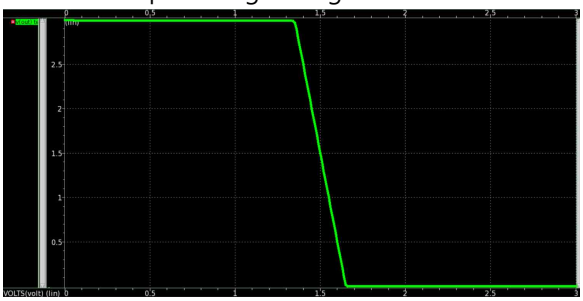
2-3 Simulation Result

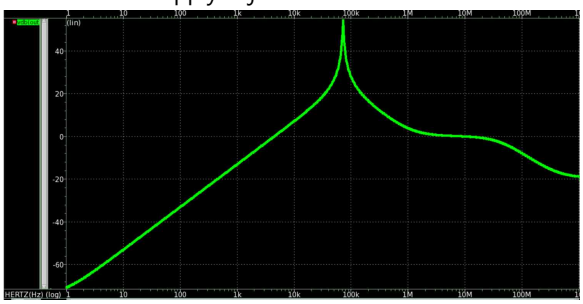
Input common-mode voltage range simulation



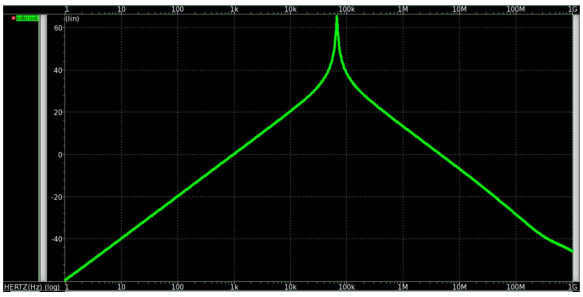
Output voltage swing simulation



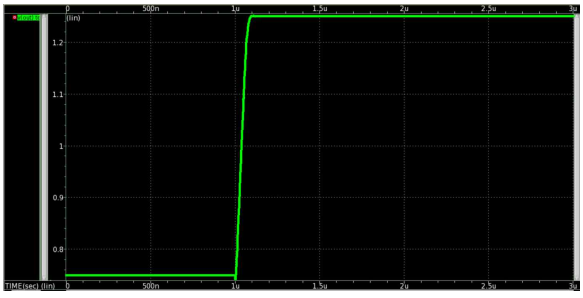
Power supply rejection ratio simulation



Common-mode rejection ratio



Slew rate and settling time



Gain, Bandwidth, Power dissipation, Phase Margin, ICMR, Output swing, PSRR, CMRR, settling time은 아래와 같이 design하였고 simulation 결과 spec을 만족시켰다.

(1) $Gain = 20\log_{10} g_{m2}(r_{O2} \parallel r_{O4}) \times g_{m6}(r_{O6} \parallel r_{O7})$
$= 20\log_{10}(2g_{m2}g_{m6}/(I_5 I_6(\lambda_2+\lambda_4)(\lambda_6+\lambda_7))$
$= 20\log_{10}(60u \times (1/170n \parallel 1/680n))$
$\times (360u \times (1/1u \parallel 1/4u) = 74.1dB$

(2) $GB = g_{m1}/2\pi C_c = 60u/(1p \times 2\pi) = 9.5MHz$

(3) $P = V_{DD} \times (I_{M5,\,M7}) = 3 \times (8u + 24u) = 96u\,W$

(4) $ICMR_{\max} = V_{DD} - V_{gsM4} = 3 - 0.1 = 2.9\,V$
$ICMR_{\min} = V_{d\,SatM1,M3,M5} - V_{gsM1}$
$= 0.1 + 0.1 + 0.1 - 0.1 = 0.2\,V$

(5) $Swing = V_{DD} - V_{od\,M1,M3,M5} = 3 - 0.3 = 2.7\,V$

(6) $PSRR^+ = \dfrac{V_{dd}}{V_{out}}$
$= \dfrac{g_{mI}g_{mII}}{G_I g_{ds6}} \times \dfrac{(sc_c/g_{mI}+1)(sc_c/g_{mII}+1)}{sg_{mII}c_c/G_I g_{ds6}+1}$
$\simeq 20\log_{10}\dfrac{60u \times 360u}{(170n+680n)\times 1u} = 88dB$
$PSRR = 20\log_{10}(\Delta V/\Delta V_{out} \times A_V)dB$
$= PSRR^+ + A_v = 88dB$

(7) $CMRR = A_{DM}/A_{CM} = 80.8dB$
$A_{DM} = g_{m2}(r_{O2} \parallel r_{O4}) \times g_{m6}(r_{O6} \parallel r_{O7}) = 44.1dB$
$A_{CM} = \dfrac{1}{1/2g_{m2}+R_{ss}} \times (1/g_{m4} \parallel r_{o4}/2 \parallel 1/g_{m6} \parallel r_{o6}/2)$
$= \dfrac{1}{1/100u+1/2u} \times (1/60u \parallel 1/1.36u \parallel$
$1/360u \parallel 1/2u) = -36.7dB$

(8) $\tau = V/SR = C_t V/I_5 = 0.5 \times 1p/8u = 62.5ns$

Ⅲ. Folded Cascode op amp

3-1 Target and result of parameters

Parameter	Target	Achievement
DC Gain	≥70dB	71.9dB
Common-Mode Input Range	1V	1.2V
OutputSwing	1V	2.2V
PowerDissipation (excludebiasing)	100uW	90.4uW
Unity GainFrequency	8MHz	14.7MHz
Settling Time (0.5V OutputStep)	100nsec to 0.1%	70nec
CMRR at DC	≥70dB at DC	82.9dB
PSRR	≥70dB at DC	82.5dB
Load Capacitance	1pF	1pF
Supply Voltage	3.3V(VDD), 0V(VSS)	3.0V(VDD), 0V(VSS)
Phase Margin	60 °	79 °

3-2 Design and Hand calculation

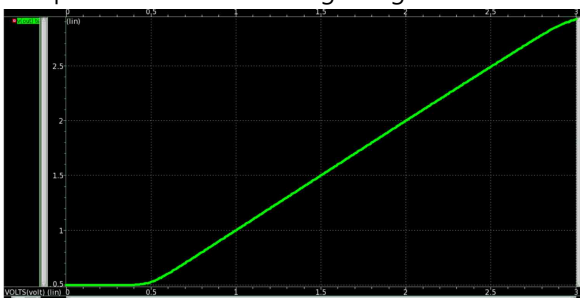
Folded cascode op amp는 위와 같이 design 하였다. 350nm 공정에서의 Nmos와 Pmos의 $u_n cox$의 값을 가지고 g_m/i_d methodology를 이용하였다. g_m/i_d를 통하여 Vod를 $100 \sim 200mv$로 설정한 후 w/l를 구하고 m, r, c의 값을 추후 다른 spec에 맞도록 계산한 후 결정하였다.

그 결과 parameter들이 아래와 같이 결정되었다.

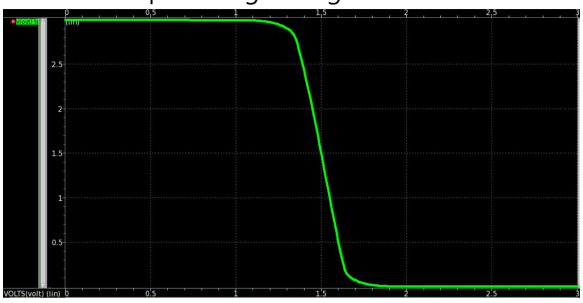
M1	l=0.7u w=0.4u m=6	M2	l=0.7u w=0.4u m=6
M3	l=0.7u w=0.4u m=12	M4	l=0.7u w=0.4u m=36
M5	l=0.7u w=0.4u m=36	M6	l=0.7u w=0.4u m=18
M7	l=0.7u w=0.4u m=18	M8	l=0.7u w=0.4u m=3
M9	l=0.7u w=0.4u m=3	M10	l=0.7u w=0.4u m=3
M11	l=0.7u w=0.4u m=3	M12	l=0.7u w=0.4u m=12
M11	l=0.7u w=0.4u m=12	M14	l=0.7u w=0.4u m=36
M15	l=0.7u w=0.4u m=36		
c_c	0pF	c_L	1pF
V_{DD}	3V	V_{ss}	0V
Ibias	15uA	R_f	0Ω
vin1	1V	vin2	1V

3-3 Simulation Result

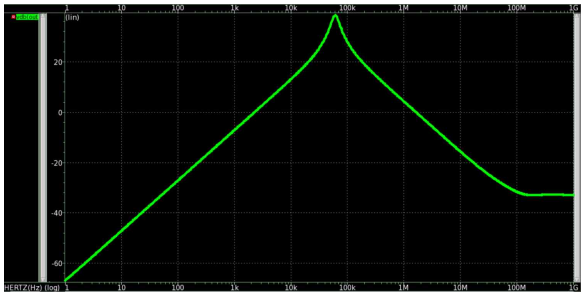
Input common-mode voltage range simulation



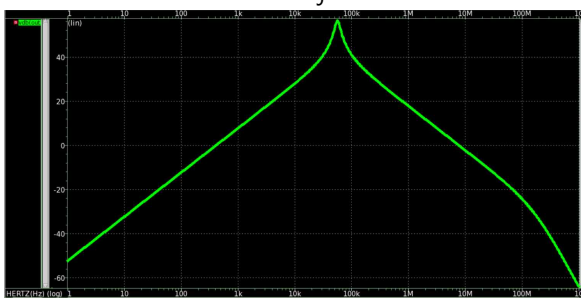
Output voltage swing simulation



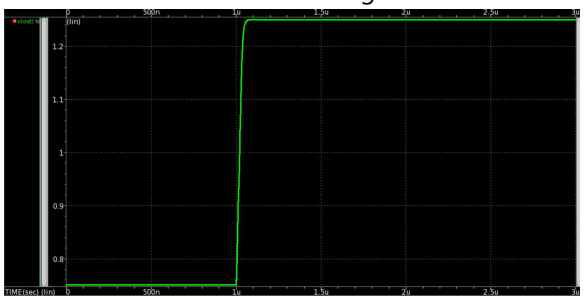
Power supply rejection ratio simulation



Common-mode rejection ratio



Slew rate and settling time



Gain, Bandwidth, Power dissipation, Phase Margin, ICMR, Output swing, PSRR, CMRR, settling time은 아래와 같이 design하였고 simulation 결과 spec을 만족시켰다.

(1) $Gain = 20\log_{10} g_{m2} \times ([g_{m7} \times r_{O7}(r_{O5} \parallel r_{O2})] \parallel [g_{m9}(r_{O9} \times r_{O11})]) = 20\log_{10}(100u \times (100u \times 1/2u \times (1/1.3u \parallel 1/100n) \parallel (100u \times 1/200n \times \times 1/200n)) = 70.1dB$

(2) $GB = g_{m1}/C_c = 100u/(1p \times 2\pi) = 16MHz$

(3) $P = V_{DD} \times (I_{M3,\,M10,\,M11})$
$= 3 \times (15u + 7.5u + 7.5u) = 90u\,W$

(4) $ICMR_{\max} = V_{DD} - V_{gsM5,7} = 3 - 1 = 2\,V$
$ICMR_{\min} = V_{dSatM9,M11,M7} - V_{gsM7}$
$= 1.15 - 0.45 = 0.7\,V$

(5) $Swing = V_{DD} - V_{od\,M4,M6,M8,M10}$
$= 3 - 0.1 - 0.1 - 0.2 - 0.2 = 2.4\,V$

(6) $PSRR^+ = \dfrac{V_{dd}}{V_{out}}$
$= \dfrac{g_{mI}g_{mII}}{G_I g_{ds6}} \times \dfrac{(sc_c/g_{mI}+1)(sc_c/g_{mII}+1)}{sg_{mII}c_c/G_I g_{ds6}+1}$
$\simeq 20\log_{10}\dfrac{100u \times 100u}{(0.1+1.3)u \times (1.8+0.4)u} = 70.2dB$
$PSRR = 20\log_{10}(\Delta V/\Delta V_{out} \times A_V)dB$
$= PSRR^+ + A_v = 70.2dB$

(7) $CMRR = A_{DM}/A_{CM} = 78.2dB$
$A_{DM} = 20\log_{10} g_{m2} \times ([g_{m7} \times r_{O7}(r_{O5} \parallel r_{O2})] \parallel [g_{m9}(r_{O9} \times r_{O11})]) = 20\log_{10}(100u \times (100u \times 1/2u \times (1/1.3u \parallel 1/100n) \parallel (100u \times 1/200n \times \times 1/200n)) = 40.1dB$
$A_{CM} = \dfrac{1}{1/2g_{m2} + R_{ss}} \times (1/g_{m7} \parallel r_{o7}/2 \parallel 1/g_{m9,m10} \parallel r_{o9,o10}/2)$
$= \dfrac{1}{1/200u + 1/2u} \times (1/60u \parallel 1/1.36u \parallel 1/360u \parallel 1/2u) = -38.1dB$

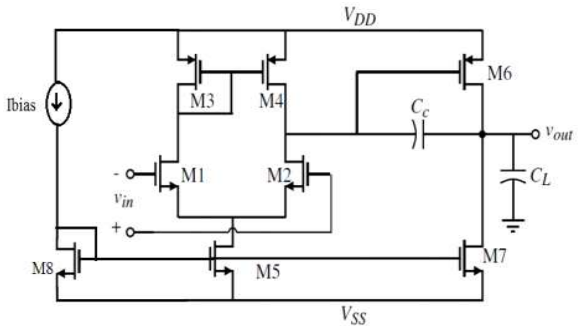
(8) $\tau = V/SR = C_t V/I_3 = 0.5 \times 1p/15u = 33.3ns$

IV. Widebandwidth op amp

4-1 Target and result of parameters

Parameter	Target	Achievement
DC Gain	≥70dB	71.1dB
Common-Mode Input Range	0.8~2.5V	1.5V
OutputSwing	0.35~2.95V	2.3V
PowerDissipation (excludebiasing)	500uW	498uW
Unity GainFrequency	140MHz	140.1MHz
Settling Time (0.5V OutputStep)	38nsec to 0.1%	40nec
CMRR at DC	≥60dB at DC	66.1dB
PSRR	≥60dB at DC	76.1dB
Load Capacitance	1pF	1pF
Supply Voltage	3.3V(VDD), 0V(VSS)	3.0V(VDD), 0V(VSS)
Phase Margin	60 °	60.4 °

4-2 Design and Hand calculation



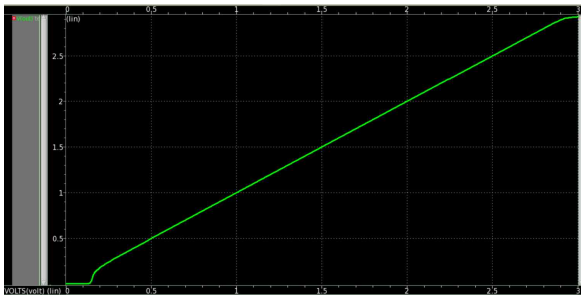
Widebandwidth op amp는 위와 같이 Two stage op amp로 design 하였다. 처음에는 two stage folded cascode로 설계하였지만 느렸고 two stage cascode으로 설계하였을 때 spec을 만족시켰지만 cascode를 안해도 spec을 만족 가능하다고 판단되어 위와 같은 기본적인 two stage op amp로 설계하였다. 350nm 공정에서의 Nmos와 Pmos의 $u_n cox$의 값을 가지고 g_m/i_d methodology를 이용하였다. g_m/i_d를 통하여 Vod를 $200 \sim 300mv$로 설정한 후 w/l를 구하고 m, r, c의 값을 추후 다른 spec에 맞도록 계산한 후 결정하였다.

그 결과 parameter들이 아래와 같이 결정되었다.

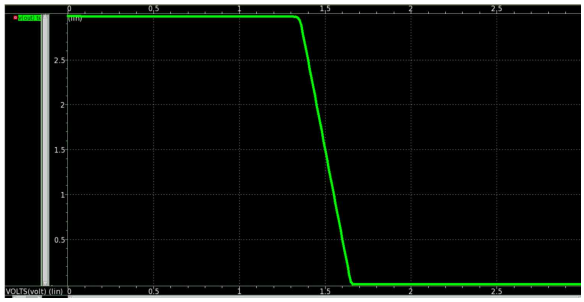
M1	l=0.55u w=0.35u m=7	M2	l=0.55u w=0.35u m=7
M3	l=0.55u w=0.35u m=21	M4	l=0.55u w=0.35u m=21
M5	l=0.55u w=0.35u m=14	M6	l=0.55u w=0.35u m=42
M7	l=0.55u w=0.35u m=17	M8	l=0.55u w=0.35u m=7
c_c	0.5pF	c_L	1pF
V_{DD}	3V	V_{ss}	0V
Ibias	20.5uA	R_f	8.2Ω
vin1	1V	vin2	1V

4-3 Simulation Result

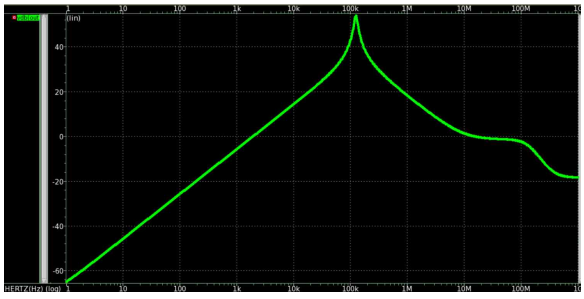
Input common-mode voltage range simulation



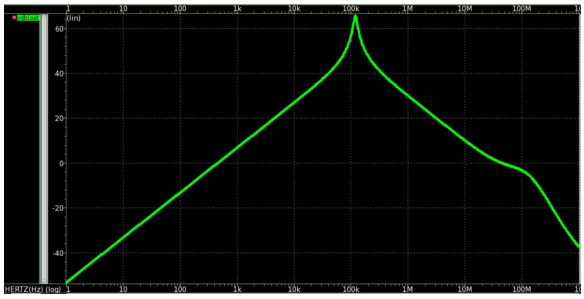
Output voltage swing simulation



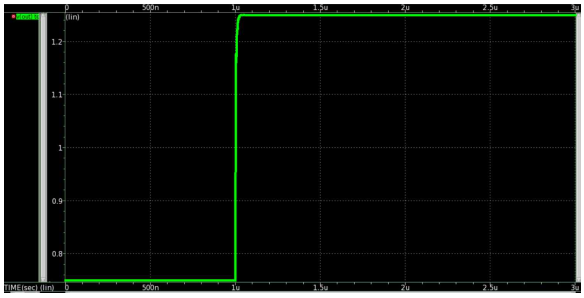
Power supply rejection ratio simulation



Common-mode rejection ratio



Slew rate and settling time



Gain, Bandwidth, Power dissipation, Phase Margin, ICMR, Output swing, PSRR, CMRR, settling time은 아래와 같이 design하였고 simulation 결과 spec을 만족시켰다.

(1) $Gain = 20\log_{10} g_{m2}(r_{O2} \parallel r_{O4}) \times g_{m6}(r_{O6} \parallel r_{O7})$
$= 20\log_{10}(2g_{m2}g_{m6}/(I_5 I_6(\lambda_2+\lambda_4)(\lambda_6+\lambda_7))$
$= 20\log_{10}(480u \times (1/1.4u \parallel 1/5.6u))$
$\times (2.9m \times (1/8u \parallel 1/32u) = 73.9dB$

(2) $GB = g_{m1}/C_c = 480u/(0.5p \times 2\pi) = 152MHz$

(3) $P = V_{DD} \times (I_{M5,\,M7}) = 3(40+120)u = 480u\,W$

(4) $ICMR_{\max} = V_{DD} - V_{gsM4} = 3-1 = 2\,V$
$ICMR_{\min} = V_{d\,SatM1,\,M3,\,M5} - V_{gsM1}$
$= 1-0.2+0.2+0.2 = 0.4\,V$

(5) $Swing = V_{DD} - V_{od\,M1,\,M3,\,M5} = 3-0.6 = 2.4\,V$

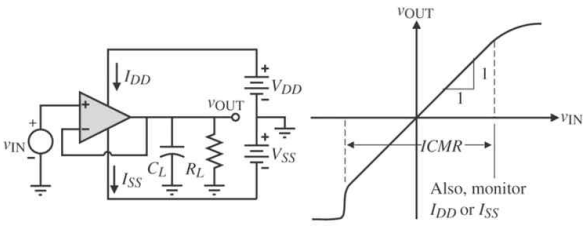
(6) $PSRR^{+} = \dfrac{V_{dd}}{V_{out}}$
$= \dfrac{g_{mI}g_{mII}}{G_I g_{ds6}} \times \dfrac{(sc_c/g_{mI}+1)(sc_c/g_{mII}+1)}{sg_{mII}c_c/G_I g_{ds6}+1}$
$\simeq 20\log_{10}\dfrac{480u \times 2.9m}{(1.4u+5.6u)\times 8u} = 87.9dB$
$PSRR = 20\log_{10}(\Delta V/\Delta V_{out} \times A_V)dB$
$= PSRR^{+} + A_v = 88 = 87.9dB$

(7) $CMRR = A_{DM}/A_{CM} = 80.8dB$
$A_{DM} = g_{m2}(r_{O2} \parallel r_{O4}) \times g_{m6}(r_{O6} \parallel r_{O7}) = 44.1dB$
$A_{CM} = \dfrac{1}{1/2g_{m2}+R_{ss}} \times (1/g_{m4} \parallel r_{o4}/2 \parallel 1/g_{m6} \parallel r_{o6}/2)$
$= \dfrac{1}{1/800u+1/16u} \times (1/480u \parallel 1/10.9u \parallel$
$1/2.9m \parallel 1/16u) = -36.7dB$

(8) $\tau = C_c V/I_5 = 0.5 \times 1.5p/40u = 18.8ns$

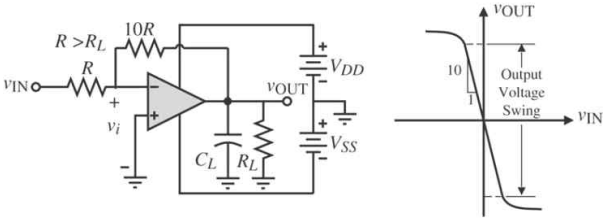
V Ways to Measure Parameters with simulation

5-1 Input common-mode voltage range simulation



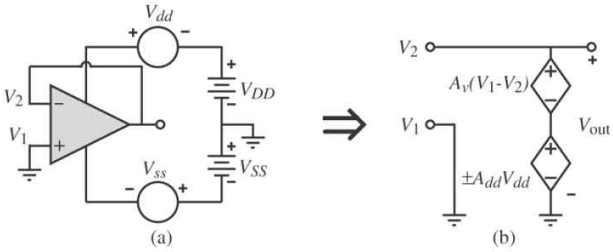
ICMR은 Unit gain Buffer을 구성한 후 input을 VSS에서 VDD까지 sweep한다.

5-2 Output voltage swing simulation



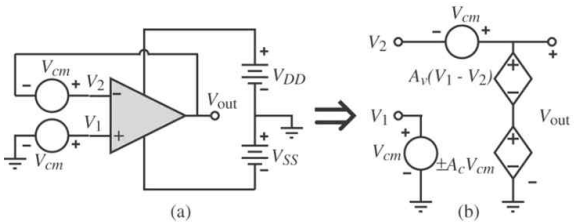
Output Voltage swing은 Unit gain Buffer을 구성한 후 input을 VSS에서 VDD까지 sweep한다.

5-3 Power supply rejection ratio simulation



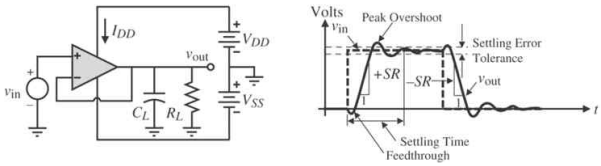
PSRR은 Unit gain amp를 구성한 후 VDD에 AC를 주면 PSRR+, VSS에 AC를 주면 PSRR-를 구한다. PSRR+의 정의가 V_{DD}/V_{out}이고 PSRR의 정의가 $20\log_{10}(\Delta V / \Delta V_{out} \times A_V)dB$

5-4 Common-Mode Rejection Ratio simuulation



CMRR은 아래와 같이 구성한 후 amp에 feedback을 걸고 입력에 pulse를 인가한다. 이때 0.5V를 output step를 가져야하므로 필자는 1.25V에서 1.75V의 pulse를 인가하였다. CMRR의 정의가 V_{cm}/V_{out}임을 이용하여 구한다.

5-5 Common-Mode Rejection Ratio simuulation



Slew rate은 Unit gain amp를 구성한 후 V2의 Vcm에 AC를 주고 V1의 Vcm은 DC와 AC를 준다. 이때 CMRR의 정의가 V_{out}/V_{DD}이다.

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